REMARKS

The objections, rejections and comments of the Examiner set forth in the Office Action dated September 3, 2003 have been carefully reviewed by the Applicants.

The drawings are objected to under 37 CFR 1.83(a) for failing to show every feature specified in the Claims. Specifically, the drawings fail to show a page buffer and pre-charge registers. In response, Figure 6 has been amended to show pre-charge buffers 624 within flash memory 620, and a page buffer 622 within RAM 622. Support for the amendment of Figure 6 is provided at page 4, lines 14-17, and at page 13m lines 9-12. An amended Figure 6 is attached.

Claims 20 and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, there is insufficient antecedent basis for "said device." In response, Claim 20 has been canceled, and "said device" in Claim 21 has been changed to "said first multi level cell flash memory."

Claims 1, 6 and 14 are currently rejected under 35 U.S.C. 102(b) as being anticipated by Hasbun et al. (US 5936884). Claims 2, 7-13, 15-25 are currently rejected under 35 U.S.C. 103(a) as being unpatentable over Hasbun et al. (US 5936884). Claim 3 is currently rejected under 35 U.S.C. 103(a) as being unpatentable over Hasbun et al. (US 5936884) in view of Im (US 2003/0016562).

In response to the above rejections, independent Claims 1, 6, 14, 18 and 19 have been amended to patentably distinguish the present claimed invention from Hasbun and the combination of Hasbun and Im. Claims 7, 10, 20, and 23 have been canceled.

Claim 1 has been amended to recite a multi-level memory cell having one erased state and three programmed states that is programmable by writing two bits of information to the cell. As taught by Hasbun, a multi-level memory cell having one erased state and three programmed states would be programmed by writing one bit of information, not two.

Hasbun teaches the partitioning of storage levels into groups and writing a number of bits into a group that is less than the maximum number of bits that could normally be written into the

cell. Hasbun achieves sequential writes without erasing by logically subdividing a multi-level cell into a number logical cells that are sequentially written to until they have all been programmed. After all of the logical cells have been programmed, they are renewed by erasing the physical memory cell containing the logical cells.

Claim 6 has been amended to recite reading existing cell storage conditions from said device and combining said existing cell storage conditions with programming information to produce new information. Hasbun does read existing cell storage conditions and combine with programming information. Hasbun relies on a "tracking mechanism" " (column 4, lines 4-45) or "group indicator" (column 8, lines 59-67) to determine the level or levels for programming.

Claim 14 has been amended to recite a multi-level memory cell having one erased state and three programmed states that is programmable by writing two bits of information to the cell. As taught by Hasbun, a multi-level memory cell having one erased state and three programmed states would be programmed by writing one bit of information, not two.

Claim 18 has been amended to recite a multi-level memory cell having one erased state and three programmed states that is programmable by writing two bits of information to the cell. As taught by Hasbun, a multi-level memory cell having one erased state and three programmed states would be programmed by writing one bit of information, not two.

Claim 19 has been amended to recite reading existing cell storage conditions from said device and combining said existing cell storage conditions with programming information to produce new information;. Hasbun does read existing cell storage conditions and combine with programming information. Hasbun relies on a "tracking mechanism" " (column 4, lines 4-45) or "group indicator" (column 8, lines 59-67) to determine the level or levels for programming.

Independent Claims 1, 6, 14, 18 and 19 have been amended to include a limitation that is neither taught nor suggested by Hasbun and Im, separately or in combination. In summary, Applicant assert that Claims 1-6, 8-9, 11-19, 21-22, and 24-25 are in condition for allowance and earnestly solicit such action by the Examiner.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,

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Date: _____, 2003

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